	TET ESTEL AS ESTONIA	**April** **2016**

Series
TFI343V-500

High Frequency Inverter grade Capsule Thyristor Type TFI343V-500

Low switching losses
Low reverse recovery charge
Distributed amplified gate for high di/dt

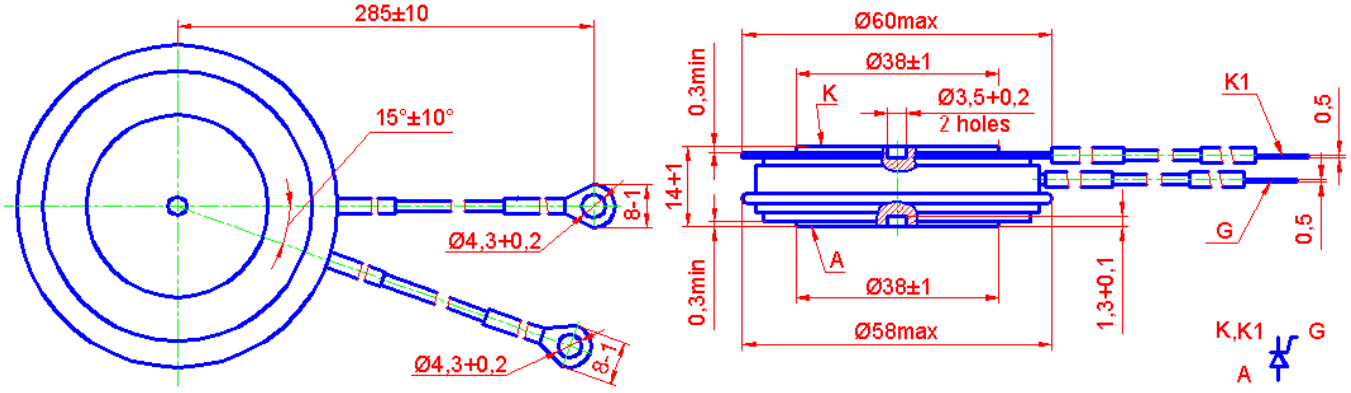
Maximum mean on-state current		**I_{TAV}**	**500 A**
Maximum repetitive peak off-state and reverse voltage		**U_{DRM}** **U_{RRM}**	**2000 ÷2400 V**
Turn-off time		**tq**	**32; 40 µs**
U_{DRM}, U_{RRM}, V	2000	2200	2400
Voltage code	20	22	24
Tvj, °C	- 60 ÷ 125		

MAXIMUM ALLOWABLE RATINGS					
Symbols and parameters		Units	TFI343V-500	Conditions	
I_{TAV}	Mean on-state current	A	500 727	Tc=83 °C, Tc=55 °C, 180° half-sine wave, 50 Hz	
I_{TRMS}	RMS on-state current	A	785	Tc=83 °C	
I_{TSM}	Surge on-state current	kA	10,0 11,0	Tvj=125°C Tvj=25°C	tp=10 ms U_R=0
I^2t	Limiting load integral	kA^2s	500 605	Tvj=125°C Tvj=25°C	
U_{DRM},U_{RRM}	Repetitive peak off-state and reverse voltage	V	2000÷2400	Tj мin≤Tvj≤Tjм 180° half-sine wave, 50 Hz Gate open	
U_{DSM},U_{RSM}	Non-repetitive peak off-state and reverse voltage	V	2100÷2500	Tj мin≤Tvj≤Tjм 180° half-sine wave tp=10 ms, Single pulse Gate open	
(di$_T$/dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/µs	 2000 1250	Tvj=125°C ; U_D=0,67 U_{DRM}, Gate pulse : 10V,5 Ω, 1µs rise time, 10 µs	
U_{RGM}	Peak reverse gate voltage	V	5	Tj мin≤Tvj≤Tjм	
Tstg	Storage temperature	°C	-60÷80		
Tvj	Junction temperature	°C	-60÷125		
CHARACTERISTICS					
U_{TM}	Peak on-state voltage	V	2,6	Tvj=25°C, I_{TM}=3,14 I_{TAV}	
$U_{T(TO)}$	Threshold voltage	V	1,6	Tvj=125°C 1,57 I_{TAV}< I_T <4,71 I_{TAV}	
R_T	On-state slope resistance	mΩ	0,69		
I_{DRM} I_{RRM}	Repetitive peak off-state and reverse current	mA	70; 70 0,7; 0,7	Tvj=125°C, U_D = U_{DRM}; U_R= U_{RRM} Tvj=25°C, U_D = U_{DRM}; U_R= U_{RRM}	

CHARACTERISTICS					
Symbols and parameters		Units	TFI343V-500	Conditions	
I_L	Latching current	A	7	Tvj=25°C,U_D=12V Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs	
I_H	Holding current	A	0,5	Tvj=25°C,U_D=12V, Gate open	
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	Tvj=25°C, Tvj=-60°C	U_D=12V
I_{GT}	Gate trigger direct current	A	0,3 0,8	Tvj=25°C, Tvj=-60°C	
U_{GD}	Gate non-trigger direct voltage	V	0,25	Tvj=125°C, U_D = 0,67 U_{DRM} Direct gate current	
I_{GD}	Gate non-trigger direct current	mA	10		
tgd	Delay time	µs	1,6	Tvj=25°C,U_D=500V I_{TM} = 500 A Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs	
tgt	Turn-on time	µs	3,2		
tq	Turn-off time	µs	32÷40 40÷50	Tvj=125°C, I_{TM} =500 A di_R/dt =10 A/µs, U_R=100V U_D = 0,67 U_{DRM} du_D/dt=50 V/µs du_D/dt=200 V/µs	
Qrr	Recovered charge	µC	400	Tvj=125°C, I_{TM} =500 A di_R/dt =50 A/µs, U_R=100V	
trr	Reverse recovery time	µs	5,5		
I_{RRM}	Peak reverse recovery current	A	145		
$(du_D/dt)_{crit}$	Critical rate of rise of off-state voltage	V/µs	500 1000	Tvj=125°C, U_D = 0,67 U_{DRM} Gate open	
Rthjc	Thermal resistance junction to case	°C/W	0,034	Direct current, double side cooled	

ORDERING								
	TFI	**343V**	**500**	**22**	**7**	**4**	**3**	
	1	**2**	**3**	**4**	**5**	**6**	**7**	

1. Fast thyristor with interdigitated gate structure.
2. Design version.
3. Mean on-state current, A.
4. Voltage code (22=2200 V).
5. Critical rate of rise of off-state voltage (6 ≥ 500 V/µs, 7 ≥1000 V/µs).
6. Group of turn-off time (du_D/dt=50 V/µs, 3 ≤ 40 µs, 4 ≤ 32 µs).
7. Group of turn-on time (2 ≤ 3,2 µs).



Mounting force : 13÷19 kN
Weight : 210 grams